REMARKS

Claims 1-75 have been been canceled. New claims 76-101 have been added. The originally-filed application supports the new claims at, for example, pgs. 7-9 and Figs. 3-5 as discussed below.

The originally-filed application referring to one exemplary embodiment disclosed by Fig. 5 states, semiconductive material layer 30 constitutes a layer from which a channel region 31 and at least one of a source region or a drain region of a thin film transistor are to be formed (pg. 8, first para.). The semiconductive material of layer 30 within contact opening 20 defines an elongated and outwardly extending channel region 31 (first para., pg. 8) (emphasis added). One of doped regions 32 of layer 30 or diffusion region 13 of bulk substrate 12 constitutes a source region of a thin film transistor, while the other of such constitutes a drain region. (2nd para., pg. 9). Region 31 constitutes a channel region, with gate layer 16 comprising an annulus which encircles thin film channel region 31 and both of channel region 31 and diffusion region 32 are elongated, with diffusion region 32 being oriented substantially perpendicular relative to channel region 31 and also substantially parallel with bulk substrate 14 (2nd para., pg. 9). Elongated channel region 31 and gate dielectric annulus 26 are perpendicularly oriented relative to bulk substrate 14 (2nd para., pg. 9).

Referring to the above disclosure and Fig. 5, the language of independent claim 76 is supported by the exemplary embodiments. Such claim recites in one example a transistor layer 30 having a channel region 31 elongated in an upward

direction and one 32 of a source region or a drain region elevationally above the channel region 31, the one region 32 comprising a structure elongated in a lateral direction substantially perpendicular to the elongated upward direction of the channel region 31 (clearly shown in Fig. 5), and the one region 32 having a dimension in the lateral direction greater than a greatest dimension of the channel region in the lateral direction (clearly shown in Fig. 5). Accordingly, claim 76 is supported by the originally-filed application.

Referring to the above disclosure and Fig. 5, the language of independent claim 86 is supported by the exemplary embodiments. Such claim in one example recites a transistor layer 30 having a thin film channel region 31, a first thin film source/drain (S/D) region 32 and a second thin film S/D region 13, the first S/D region 32 extending laterally in an elongated direction substantially parallel to surface of the substrate 12 (clearly shown in Fig. 5) and having an elongated dimension greater than a greatest dimension of the second S/D region structure 13 in a direction parallel to the surface of the substrate 12 (clearly shown in Fig. 5). Accordingly, claim 86 is supported by the originally-filed application.

Additionally, the originally-filed application referring to one exemplary embodiment of Figs. 3-4 states, gate dielectric layer 24 is anisotropically etched to define a resultant gate dielectric layer 26 within contact opening 20 laterally inward of sidewalls 22 (lines 3-5 of pg. 7), and such gate dielectric layer takes on the shape or appearance of conventional insulative sidewall spacers, and in the depicted embodiment is in the form or shape of a longitudinally elongated

annulus. Thus, electrically conductive gate layer 16 also is comprised of an annulus which surrounds contact opening 20 (lines 10-14 of pg. 7). The bulk mass of layer 16 constitutes an annulus which encircles contact opening 20. The above described process provides but one example of a manner in which a gate dielectric layer is provided within contact opening 20. Referring to Fig. 5, a layer 30 of semiconductive material is provided over second dielectric layer 18 and within contact opening 20 (lines 19-24 of pg. 7) against gate dielectric layer 26, and in electrical communication with diffusion region 13 (lines 1-2 of pg. 8).

Referring to the above disclosure and Figs. 3-5, the language of independent claim 96 is supported by the exemplary embodiments. Such claim recites in one example a second dielectric layer 18 disposed over the gate electrode layer 16 and having an upper surface (no reference number provided); an opening 20 extending from the upper surface to the semiconductor substrate 12, the opening 20 defining opposing sidewalls 22 in the gate electrode layer 16; a gate dielectric layer 26 disposed over a portion of the sidewalls 22 as an annulus (see Fig. 4), and the annulus having a top that does not extend elevationally above the upper surface (clearly shown in Fig. 5 with gate dielectric 26 not extending elevationally above the upper surface of second dielectric layer 18). Accordingly, claim 96 is supported by the originally-filed application.

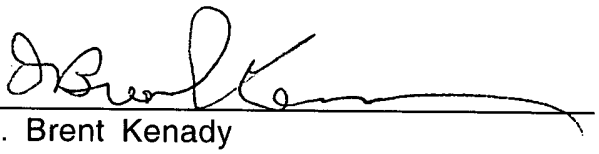
Further, Applicant herewith submits duplicate copies of the Information Disclosure Statement and Form PTO-1449 and the Supplemental Information Disclosure Statement and Form PTO-1449s filed in this application on August 1,

2001 and August 7, 2001, respectively. No initialed copy of the PTO-1449s have been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449s have not already been considered, and the Form PTO-1449s have not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449s to the undersigned.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 5-5-03

By: 

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